GaAs MMIC SLOTLINE/CPW QUADRATURE IF UPCONVERTER

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ABSTRACT

A unique GaAs monolithic Slotline/Coplanar Waveguide (SL/CPW) quadrature IF upconverter IC has been developed. The IC is a single-sideband suppressed carrier upconverter and consists of LO and RF power splitters, two IF/RF diplexers, and two SL/CPW single balanced mixers. The IC is unique because it has circuitry on both sides of the chip which required a few additional processing steps to fabricate. With a 7.0 GHz LO, and a 1 MHz to 1000 MHz quadrature IF input signal, the typical upconverter performance was 40dB LO port to RF port isolation, 25 dB carrier suppression, 20 dB sideband suppression, and 14 dB conversion loss in the 6-8 GHz RF output band.

INTRODUCTION

An image rejection upconverter was needed for a MMIC based subsystem. The requirements for the mixer were to have 30 dB LO-to-RF suppression and 25 dB sideband suppression when the LO was in the middle of the 6-8 GHz RF output band. The upconverter would mix two 0.001-1.0 GHz quadrature IF signals with a 7.0 GHz LO to derive the desired 6-8 GHz output signal. Conversion loss was not a factor in this design because the mixer was near the output stage of the subsystem. In order to meet the design specifications a unique GaAs monolithic quadrature IF upconverter has been developed.

UPCONVERTER DESIGN

The quadrature IF upconverter, shown in Figure 1, consists of LO and RF power splitters, two IF/RF diplexers, and two slotline/CPW single balanced mixers [1]. This upconverter (Figure 2) was separated into two chips because the upconverter has circuitry on both sides and could not be processed without separating the functions into two separate chips. The first chip contains the LO input port, the microstrip-to-slotline balun, the two balanced mixers, and the CPW-to-microstrip transformer. The second chip contains the IF input ports, IF/RF diplexers, the Lange coupler, and RF output ports.

The topside of the upconverter IC contains the microstrip (MS) circuitry while the bottomside contains the CPW, slotline, and the two Schottky diodes for each balanced mixer configuration.

Figure 3 shows schematics of the balanced mixer for operation in two propagation modes: 1) LO signal propagation and 2) IF/RF signal propagation. The LO signal is fed to the two balanced mixers via a MS-to-SL balun, and the quadrature IF signals are fed to the mixers through on-chip IF/RF diplexers and MS-CPW transformers [2]. The resultant output RF signals (LO ± IF) propagate from the two 180 degree balanced mixers through the IF/RF diplexers to the Lange coupler where signals from both mixers are summed. For quadrature phase IF inputs the summing process will enhance the signal level of the upper sideband signal at one RF output port and suppress the lower sideband, while the reverse is true at the other output port [3,4].

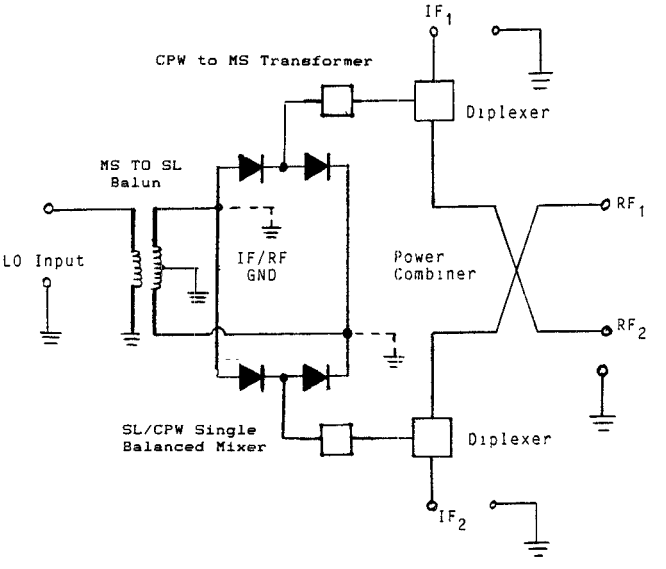

Figure 1 Quadrature IF upconverter function diagram.

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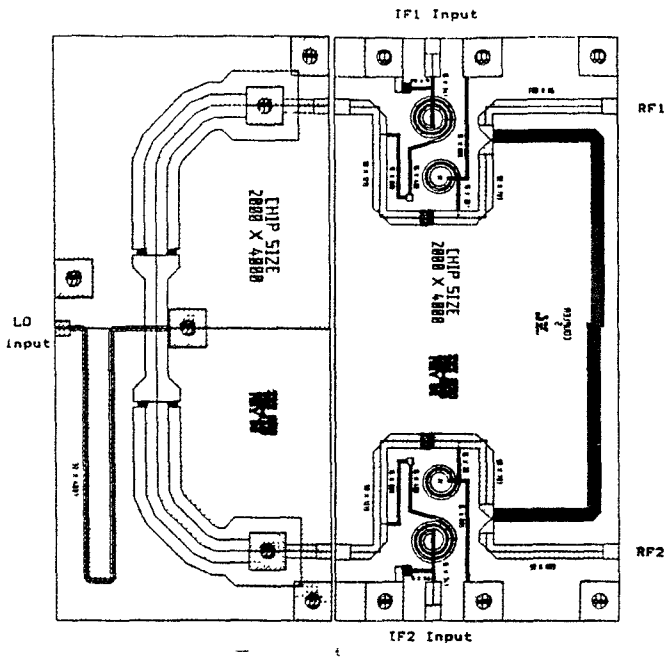

Figure 2 Quadrature IF upconverter circuit layout. Each chip is 2 mm x 4 mm.

The LO input signal propagates down a microstrip line (topside) which is terminated by a via to one of the slotline conductors (bottomside). The microstrip ground and the other slotline conductor share the same metallization. This connection (balun) transforms the microstrip transmission mode (unbalanced TEM mode) to the slotline mode (balanced TM mode). Typically for a narrowband mixer application this MS-SL balun is configured as shown in References [1,5], however, due to space limitations the balun is a modified version of the microstrip/slotline transition as described in Reference [2]. The slotline signal propagates in both directions from the via junction. The power, therefore, is divided; half propagates to one mixer and the other half propagates to the other mixer.

At each slotline-CPW plane the SL is terminated by two series connected Schottky diodes and a quarter wavelength long short circuited CPW transmission line. Actually, due to space limitations the CPW is only about one-eighth wavelength long. The impedance of each diode is about 100 ohms and the series connection is 200 ohms. Thus, the effective load for the LO signal is 100 ohms since the slotline length is small compared to the slot wave length [6,7]. A quarter wave transformer (70 ohm) was added to the LO circuit to match the 100 ohm slotline impedance to the 50 ohm microstrip impedance.

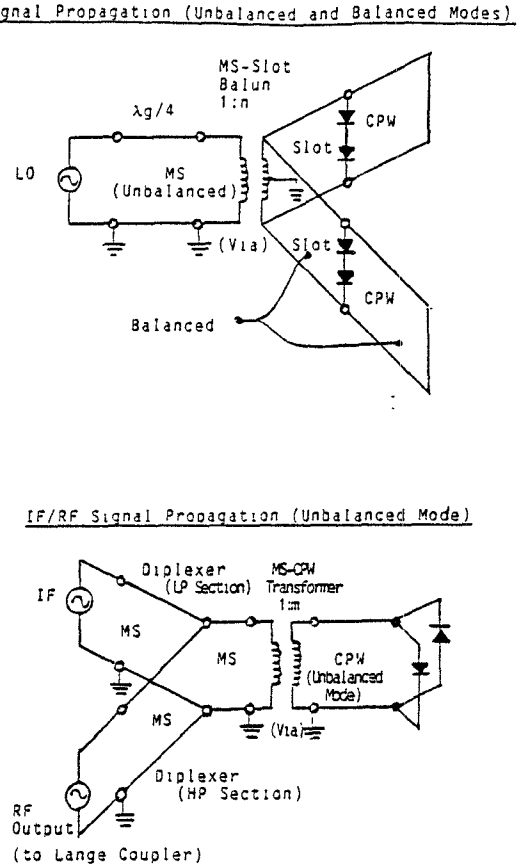

Figure 3 Propagation schematic.

The LO signal (balanced mode) is mixed with the IF signal in the Schottky diodes. The IF signal (unbalanced mode) propagates to the mixer diodes through the low pass section of the diplexer, the microstrip-to-CPW via, and the CPW 50 ohm transmission line. The summing junction between the two diodes is a virtual ground to the LO signal, therefore the LO signal does not propagate to the RF output port [8].

The RF signals (nLO ± mIF) propagate from the diode summing junction down the CPW 50 ohm transmission line through the CPW-to-microstrip via transition and the high pass section of the diplexer to the output Lange coupler. The signals from the two balanced mixers are added in the Lange coupler in such a manner so that the unwanted sideband signal (LO-IF or LO + IF) is suppressed.

Since both CPW and MS operate in odd/unbalanced modes, the transition from MS to CPW through a via (which connects both center conductors) creates a low VSWR discontinuity. The CPW-to-slotline transition, however, is an open circuit (slotline does not support an odd mode).

FABRICATION

The ICs were fabricated using the ITT Gallium Arsenide Technology Center (ITT-GTC) recessed gate microwave process for ion implanted $_{17}$GaAs. The active layer had a doping n = 1x10^{17} cm-3 and thickness t = 0.15 µm. The process includes AuGe/Ni metallization for ohmic contacts, Ti/Pd/Au Schottky gates, and Si_3N_4 overlay capacitors. The air bridges, microstrip lines, and bonding pads are 5 µm plated gold. The wafer is lapped to its final thickness of 125 µm; afterward backside via holes are etched. To insure successful processing of the circuit, two different methods are employed for backside metallization: patterned backside metal is defined using evaporated Au and liftoff techniques for the SL/CPW chip, and a backside ground plane is plated onto the microstrip chip on a separate wafer. The two chips are then mounted together on a carrier.

PACKAGING

The chips were epoxied side-by-side onto a carrier with the microstrip side up. The test fixture was designed and fabricated using standard MIC hybrid techniques with the following exception: Since the first chip had the diodes and SL/CPW circuitry on the back (down) side, it was mounted across a .031 x .210 x .050 inch deep cavity and only the chip edges were epoxied onto the carrier.

TEST RESULTS

Figure 4 shows the output spectrum of the upconverter when the IF input is 5 MHz and the phase of one port leads or lags the phase of the other port by 90 degrees. For this example the worst case LO port to RF port isolation was 44 dB.

Figure 5 shows the output spectrum when the IF signals are swept from 90 MHz to 1000 MHz (the relative phase was constant at 90 degrees offset). Note that the level of the LO signal is about 25 dB below the RF signal level, and the side band suppression is 20 dB.

Figure 6 shows the relative signal levels of the upconverter when the LO is swept from 3.0 to 12.0 GHz. The IF input signal was constant at 400 MHz. The upconverter was shown to have a broadband response even though the operating range for this application is 6-8 GHz.

The VSWR at the IF ports was better than 2.0:1, the VSWR at the RF ports was about 2.5:1, and the LO port VSWR was about 7.0:1. The design goals for the upconverter were to have the unwanted sideband suppressed greater than 25 dB and LO to RF isolation of greater than 40 dB. The typical measured performance of the SL/CPW upconverter was 20 dB and 40 dB, respectively. Table 1 summarizes the design specifications and the measured performance.

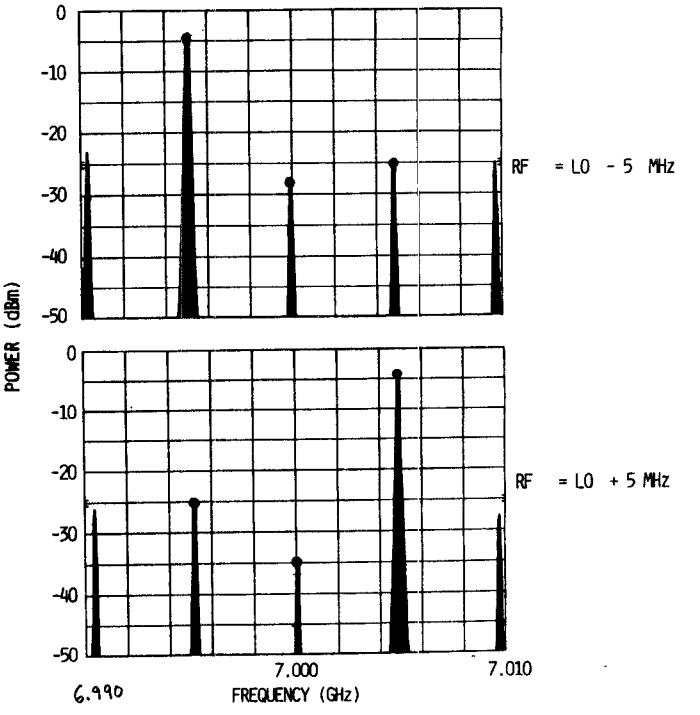

Figure 4 Output spectrum with the LO input signal at 7 GHz and 17 dBm, and the IF input signals were at 5 MHz and 7 dBm and offset by 90 degrees.

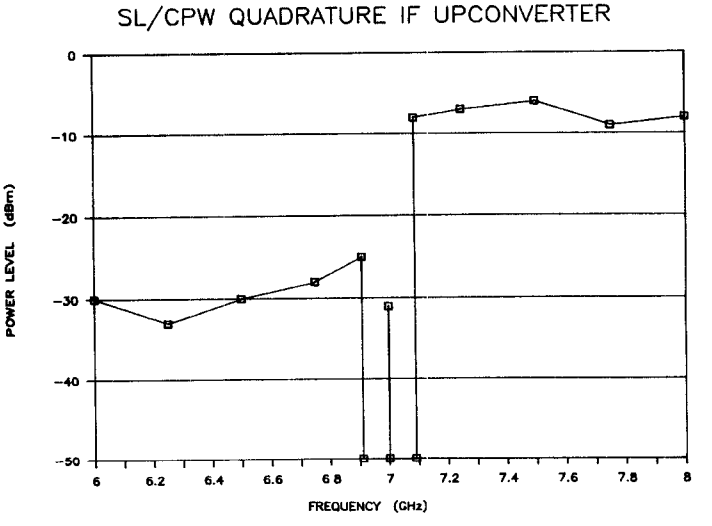

Figure 5 Output power level of each sideband as the IF frequency was swept from 90 MHz to 1000 MHz. The LO input signal was at 7 GHz and 17 dBm, and the IF input powers were 7 dBm.

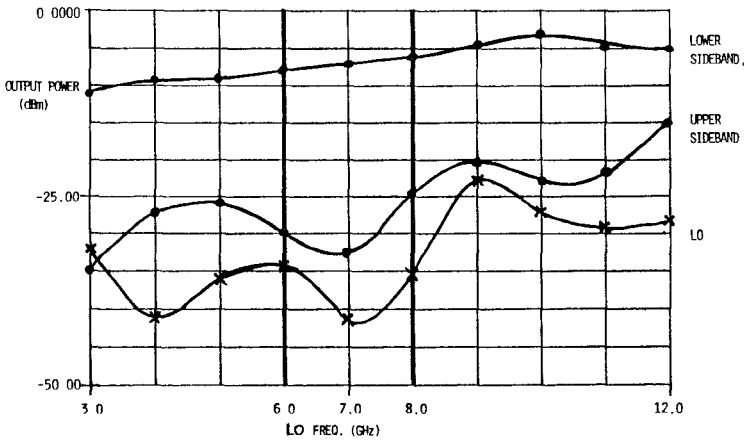

Figure 6 Output power level of the LO and each sideband as the LO frequency was swept from 3 to 12 GHz. The LO input power was 17 dBm, and the IF input powers were 7 dBm at 400 MHz and offset by 90 degrees.

Table 1

Design Specifications versus Measured Performance

UPCONVERTER

Parameters	SPECS	Measured
RF Frequency	**6-8 GHz**	**6-8 GHz**
LO Frequency	**7.0 GHz**	**7.0 GHz**
IF Frequency	**.001-1.0 GHz**	**.001-1.0 GHz**
Conversion	**8 dB Max.**	**14 dB ± 1 Typical**
LO to RF Isolation	**40 dB Min.**	**40 dB Min.**
Carrier Suppression	**30 dB Min.**	**25 dB Typical**
Sideband Suppression	**25 dB Min.**	**20 dB Typical**

CONCLUSION

A slotline/CPW quadrature IF upconverter IC has been developed which met the needs of a MMIC based subsystem. Because the IC has circuitry on both sides of the chip extra processing steps were needed to fabricate the IC.

ACKNOWLEDGMENTS

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